Fig.1

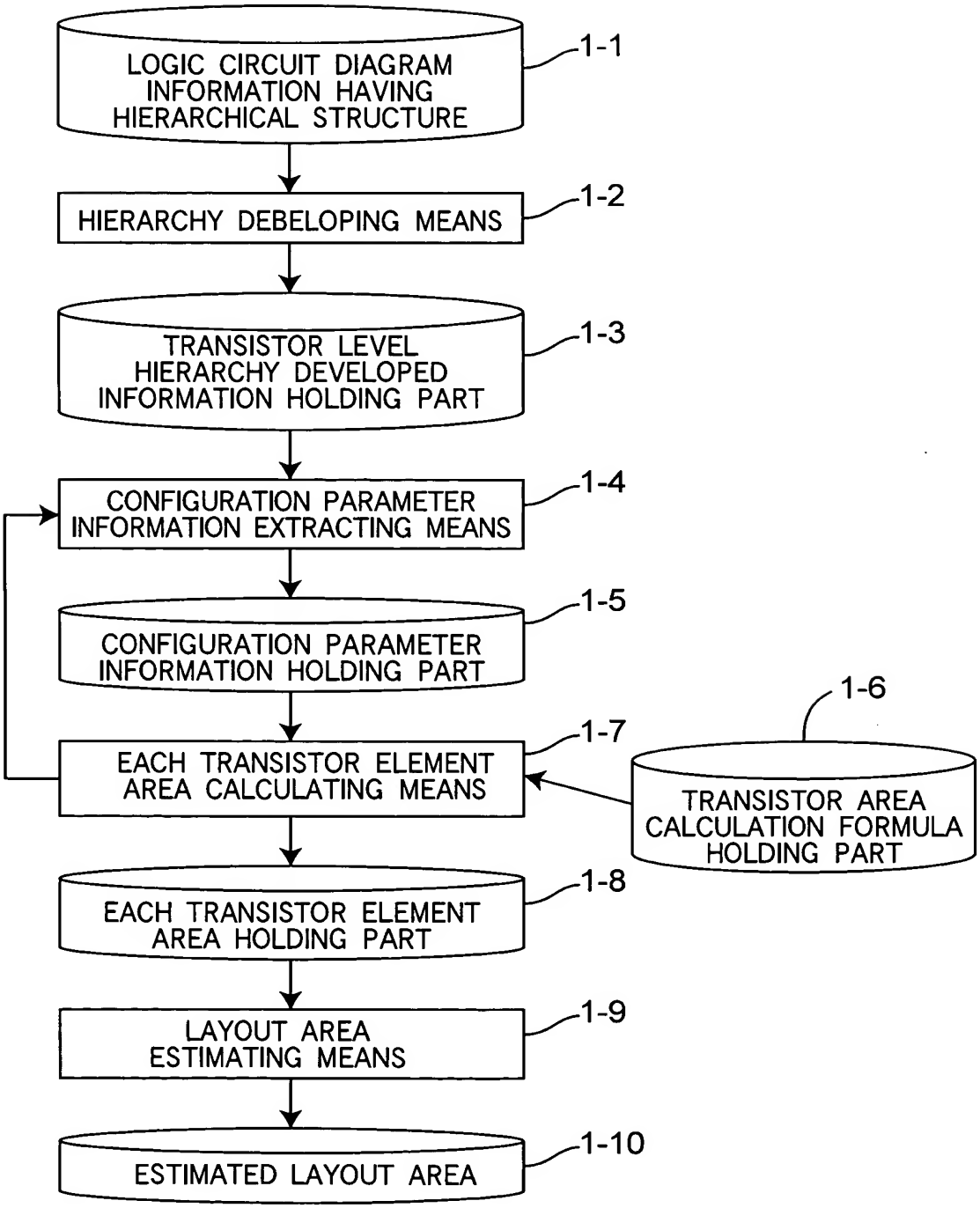

LOGIC CIRCUIT DIAGRAM INFORMATION HAVING HIERARCHICAL STRUCTURE
1-1
HIERARCHY DEBELOPING MEANS
1-2
TRANSISTOR LEVEL HIERARCHY DEVELOPED INFORMATION HOLDING PART
1-3
CONFIGURATION PARAMETER INFORMATION EXTRACTING MEANS
1-4
CONFIGURATION PARAMETER INFORMATION HOLDING PART
1-5
1-6
EACH TRANSISTOR ELEMENT AREA CALCULATING MEANS
1-7
TRANSISTOR AREA CALCULATION FORMULA HOLDING PART
EACH TRANSISTOR ELEMENT AREA HOLDING PART
1-8
LAYOUT AREA ESTIMATING MEANS
1-9
ESTIMATED LAYOUT AREA
1-10

Fig.2

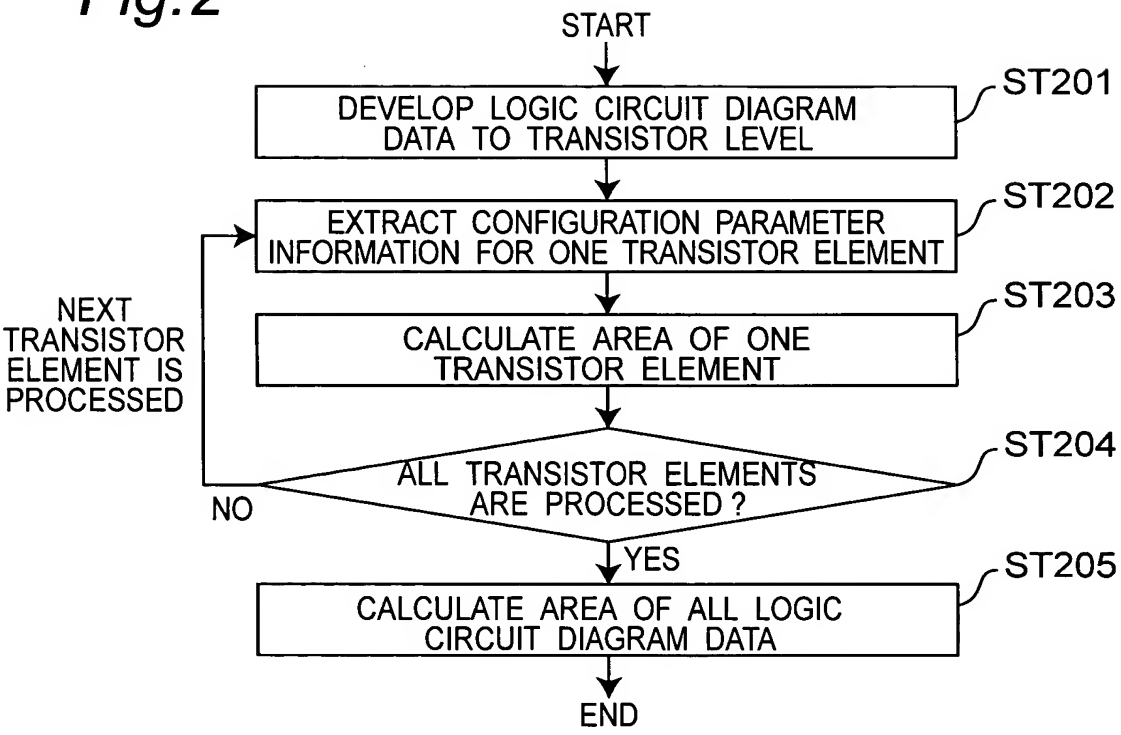

START
DEVELOP LOGIC CIRCUIT DIAGRAM DATA TO TRANSISTOR LEVEL
ST201
EXTRACT CONFIGURATION PARAMETER INFORMATION FOR ONE TRANSISTOR ELEMENT
ST202
CALCULATE AREA OF ONE TRANSISTOR ELEMENT
ST203
NEXT TRANSISTOR ELEMENT IS PROCESSED
ALL TRANSISTOR ELEMENTS ARE PROCESSED ?
ST204
NO
YES
CALCULATE AREA OF ALL LOGIC CIRCUIT DIAGRAM DATA
ST205
END

Fig.3

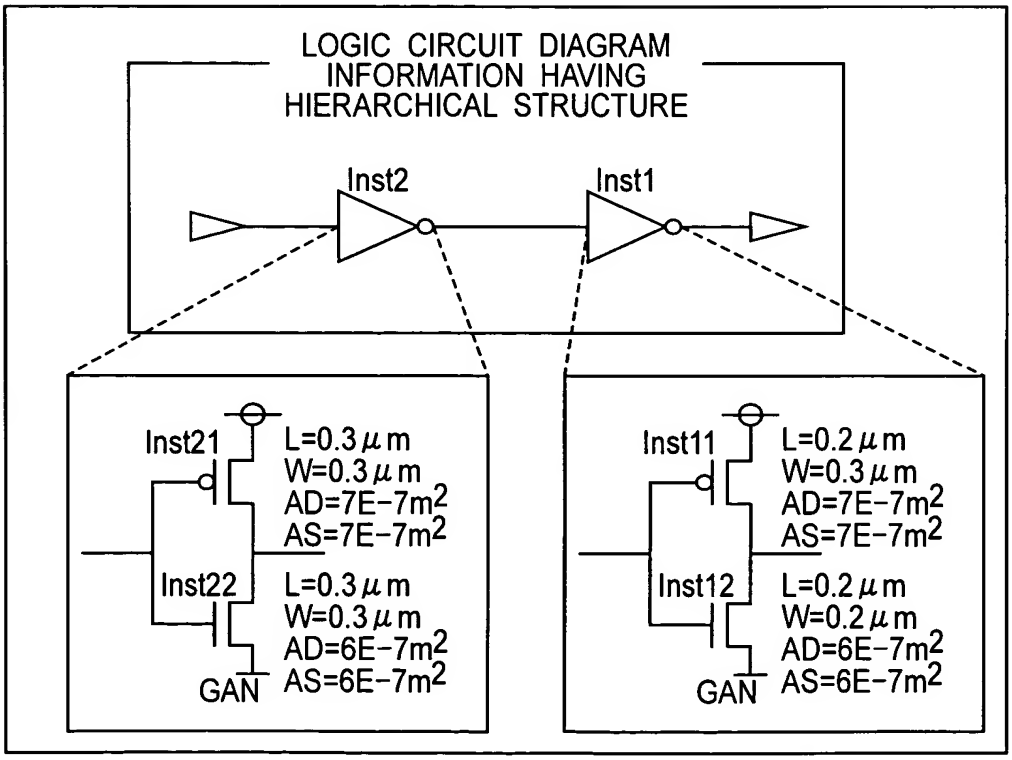

LOGIC CIRCUIT DIAGRAM INFORMATION HAVING HIERARCHICAL STRUCTURE
Inst2
Inst1
Inst21
L=0.3μm
W=0.3μm
AD=7E-7m2
AS=7E-7m2
Inst22
L=0.3μm
W=0.3μm
AD=6E-7m2
AS=6E-7m2
GAN
Inst11
L=0.2μm
W=0.3μm
AD=7E-7m2
AS=7E-7m2
Inst12
L=0.2μm
W=0.2μm
AD=6E-7m2
AS=6E-7m2
GAN

Fig.4

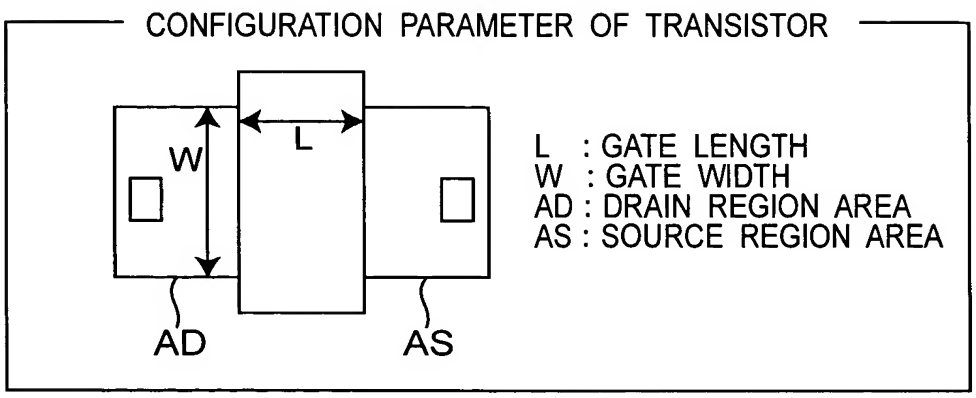

CONFIGURATION PARAMETER OF TRANSISTOR
W
L
AD
AS
L : GATE LENGTH
W : GATE WIDTH
AD : DRAIN REGION AREA
AS : SOURCE REGION AREA

Fig.5

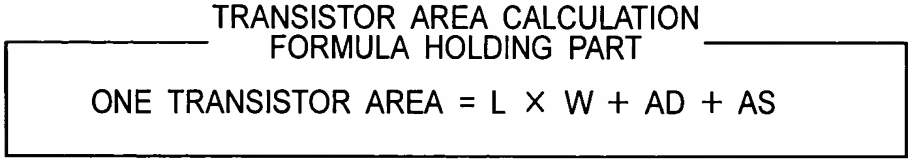

TRANSISTOR AREA CALCULATION FORMULA HOLDING PART
ONE TRANSISTOR AREA = L × W + AD + AS

Fig.6

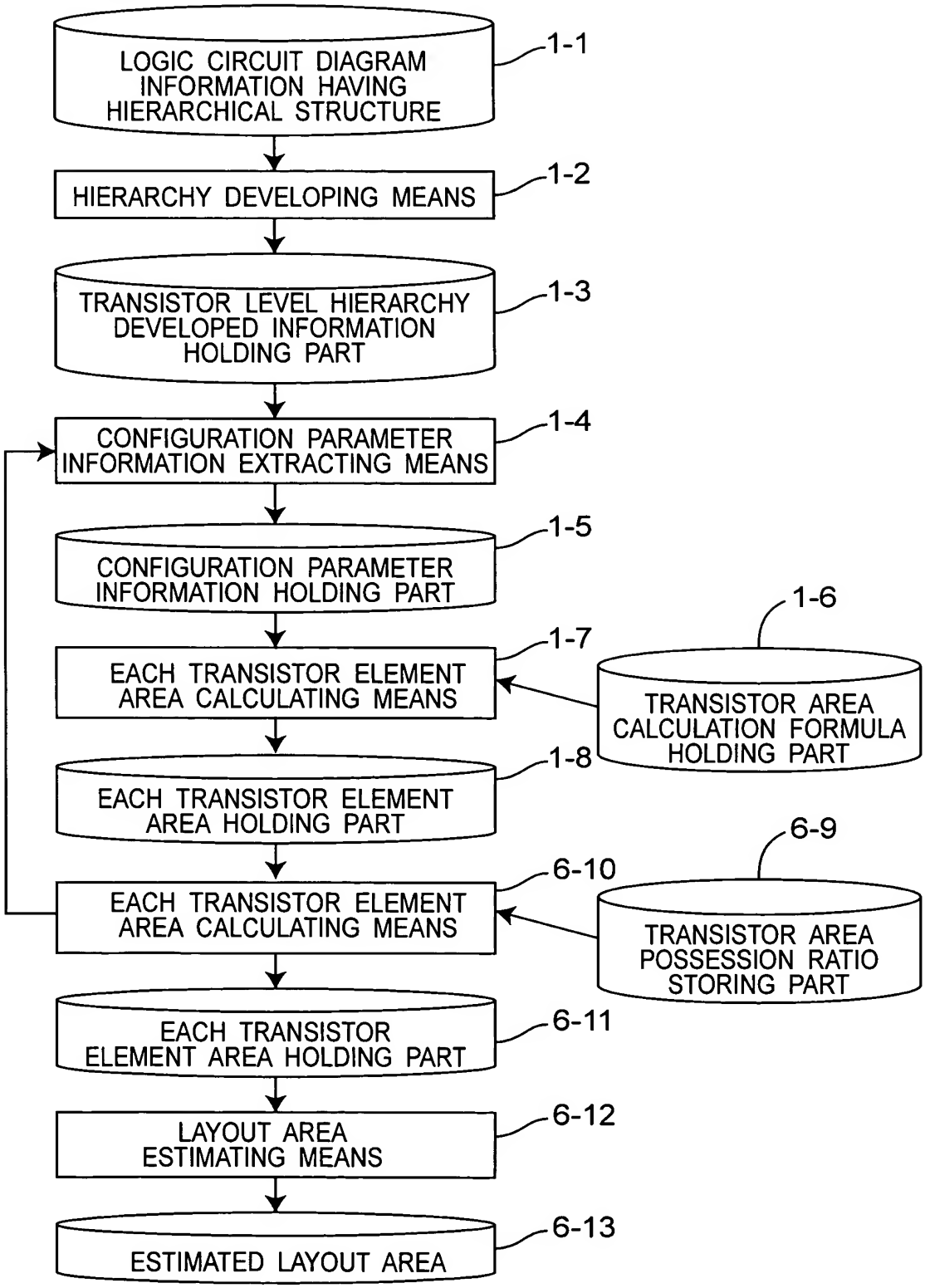

LOGIC CIRCUIT DIAGRAM INFORMATION HAVING HIERARCHICAL STRUCTURE
1-1
HIERARCHY DEVELOPING MEANS
1-2
TRANSISTOR LEVEL HIERARCHY DEVELOPED INFORMATION HOLDING PART
1-3
CONFIGURATION PARAMETER INFORMATION EXTRACTING MEANS
1-4
CONFIGURATION PARAMETER INFORMATION HOLDING PART
1-5
EACH TRANSISTOR ELEMENT AREA CALCULATING MEANS
1-7
1-6
TRANSISTOR AREA CALCULATION FORMULA HOLDING PART
EACH TRANSISTOR ELEMENT AREA HOLDING PART
1-8
EACH TRANSISTOR ELEMENT AREA CALCULATING MEANS
6-10
6-9
TRANSISTOR AREA POSSESSION RATIO STORING PART
EACH TRANSISTOR ELEMENT AREA HOLDING PART
6-11
LAYOUT AREA ESTIMATING MEANS
6-12
ESTIMATED LAYOUT AREA
6-13

Fig.7

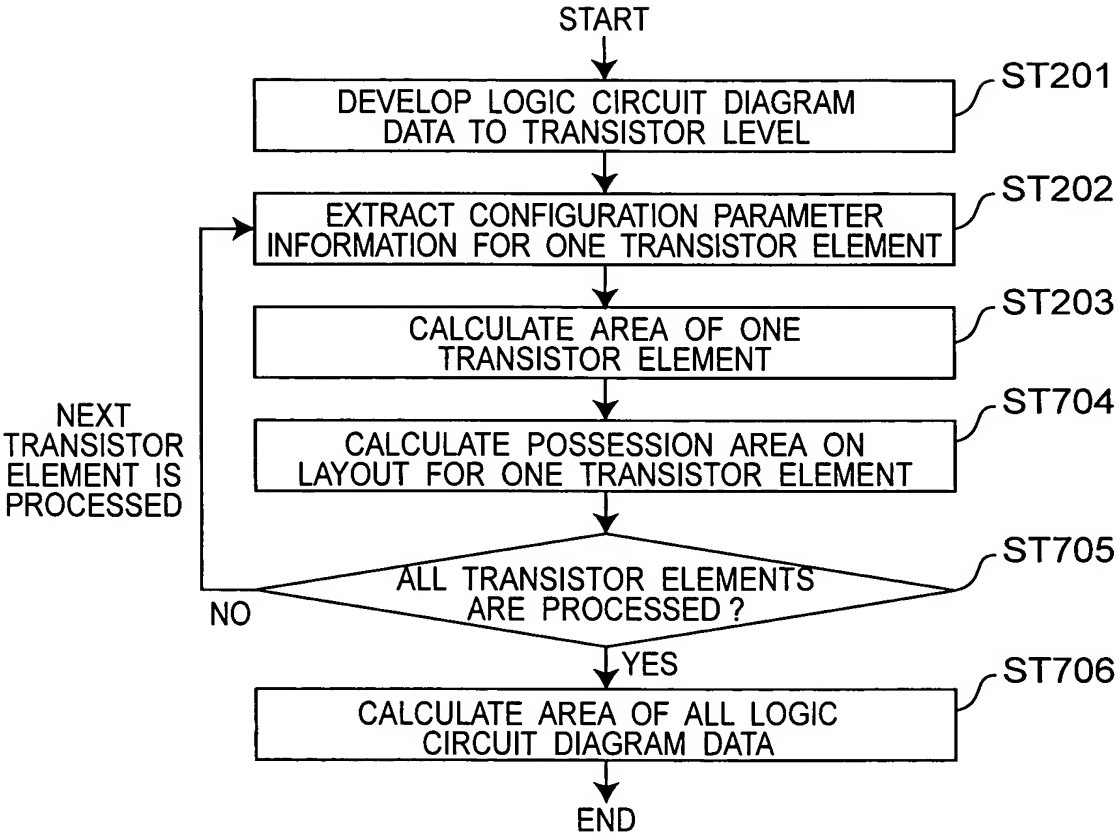

START
DEVELOP LOGIC CIRCUIT DIAGRAM DATA TO TRANSISTOR LEVEL
ST201
EXTRACT CONFIGURATION PARAMETER INFORMATION FOR ONE TRANSISTOR ELEMENT
ST202
CALCULATE AREA OF ONE TRANSISTOR ELEMENT
ST203
CALCULATE POSSESSION AREA ON LAYOUT FOR ONE TRANSISTOR ELEMENT
ST704
ALL TRANSISTOR ELEMENTS ARE PROCESSED ?
ST705
NO
NEXT TRANSISTOR ELEMENT IS PROCESSED
YES
CALCULATE AREA OF ALL LOGIC CIRCUIT DIAGRAM DATA
ST706
END

Fig.8

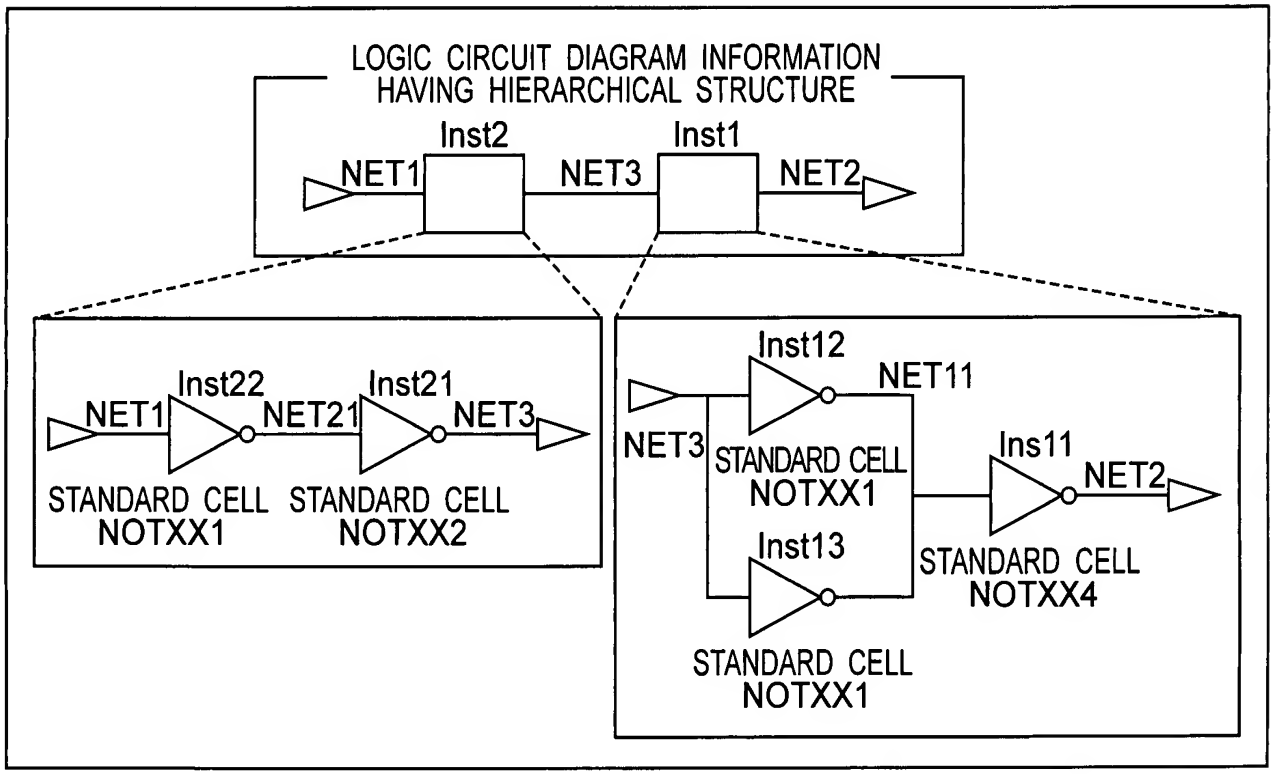

LOGIC CIRCUIT DIAGRAM INFORMATION
HAVING HIERARCHICAL STRUCTURE
Inst2
Inst1
NET1
NET3
NET2
Inst22
Inst21
NET1
NET21
NET3
STANDARD CELL
NOTXX1
STANDARD CELL
NOTXX2
Inst12
NET11
NET3
STANDARD CELL
NOTXX1
Ins11
NET2
Inst13
STANDARD CELL
NOTXX4
STANDARD CELL
NOTXX1

Fig.9

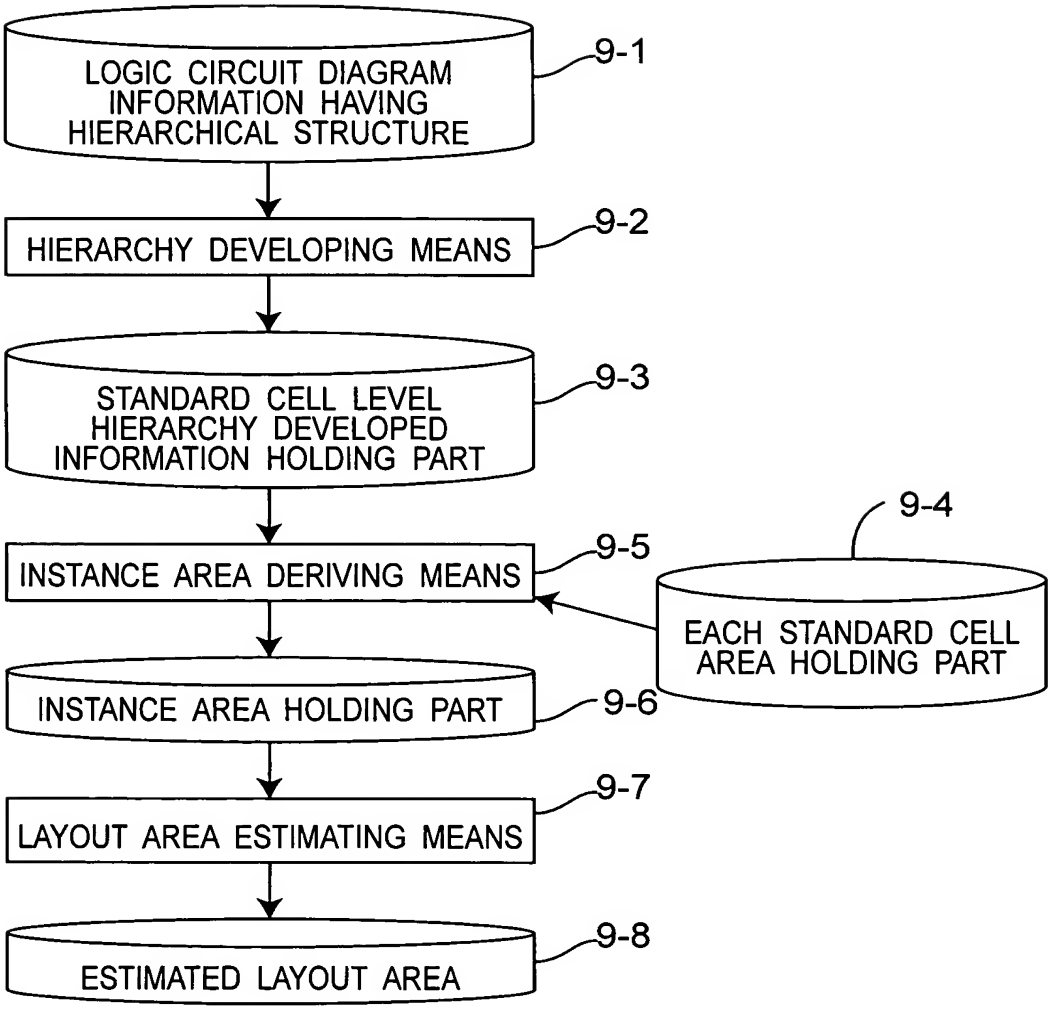

LOGIC CIRCUIT DIAGRAM INFORMATION HAVING HIERARCHICAL STRUCTURE
9-1
HIERARCHY DEVELOPING MEANS
9-2
STANDARD CELL LEVEL HIERARCHY DEVELOPED INFORMATION HOLDING PART
9-3
9-4
INSTANCE AREA DERIVING MEANS
9-5
EACH STANDARD CELL AREA HOLDING PART
INSTANCE AREA HOLDING PART
9-6
LAYOUT AREA ESTIMATING MEANS
9-7
ESTIMATED LAYOUT AREA
9-8

Fig.10

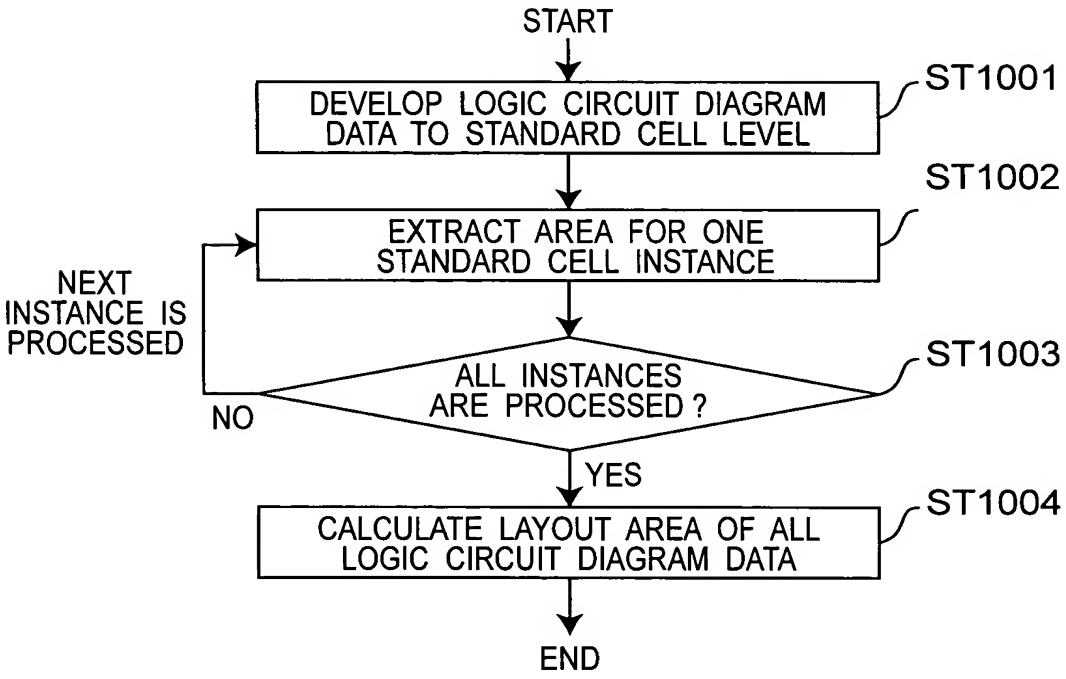


Fig.11

DEFINITION EXAMPLE OF EACH STANDARD CELL AREA HOLDING PART

NOTXX1	10E−8 μm^2
NOTXX2	20E−8 μm^2
NOTXX4	40E−8 μm^2
NOTXX8	80E−8 μm^2
⋮	⋮
⋮	⋮

Fig.12

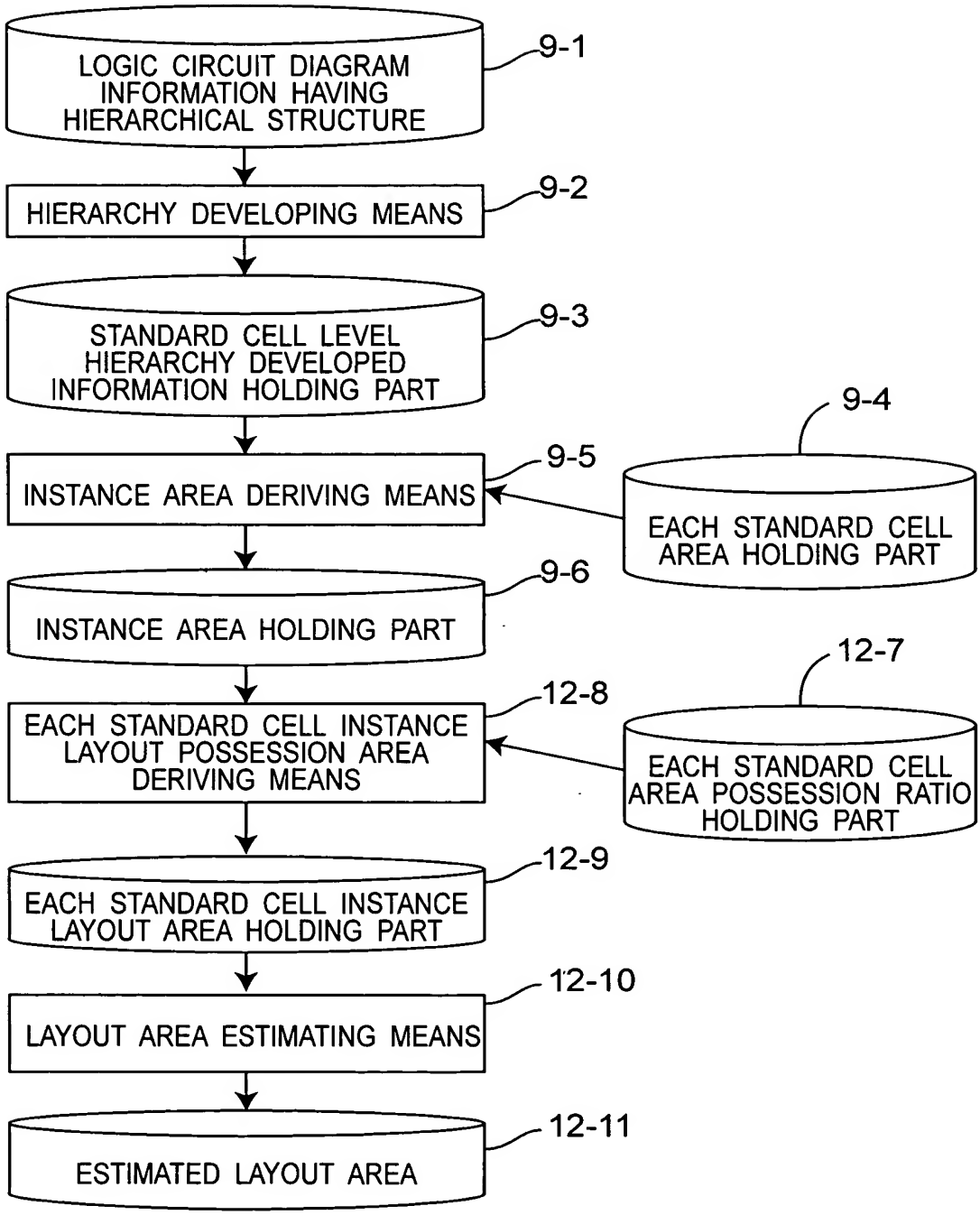

LOGIC CIRCUIT DIAGRAM INFORMATION HAVING HIERARCHICAL STRUCTURE
9-1
HIERARCHY DEVELOPING MEANS
9-2
STANDARD CELL LEVEL HIERARCHY DEVELOPED INFORMATION HOLDING PART
9-3
9-4
INSTANCE AREA DERIVING MEANS
9-5
EACH STANDARD CELL AREA HOLDING PART
INSTANCE AREA HOLDING PART
9-6
12-7
EACH STANDARD CELL INSTANCE LAYOUT POSSESSION AREA DERIVING MEANS
12-8
EACH STANDARD CELL AREA POSSESSION RATIO HOLDING PART
EACH STANDARD CELL INSTANCE LAYOUT AREA HOLDING PART
12-9
LAYOUT AREA ESTIMATING MEANS
12-10
ESTIMATED LAYOUT AREA
12-11

Fig.13

DEFINITION EXAMPLE OF EACH STANDARD CELL AREA POSSESSION RATIO HOLDING PART

NOTXX1	0.8
NOTXX2	0.9
NOTXX4	0.9
NOTXX8	0.8
:	:
:	:

Fig.14

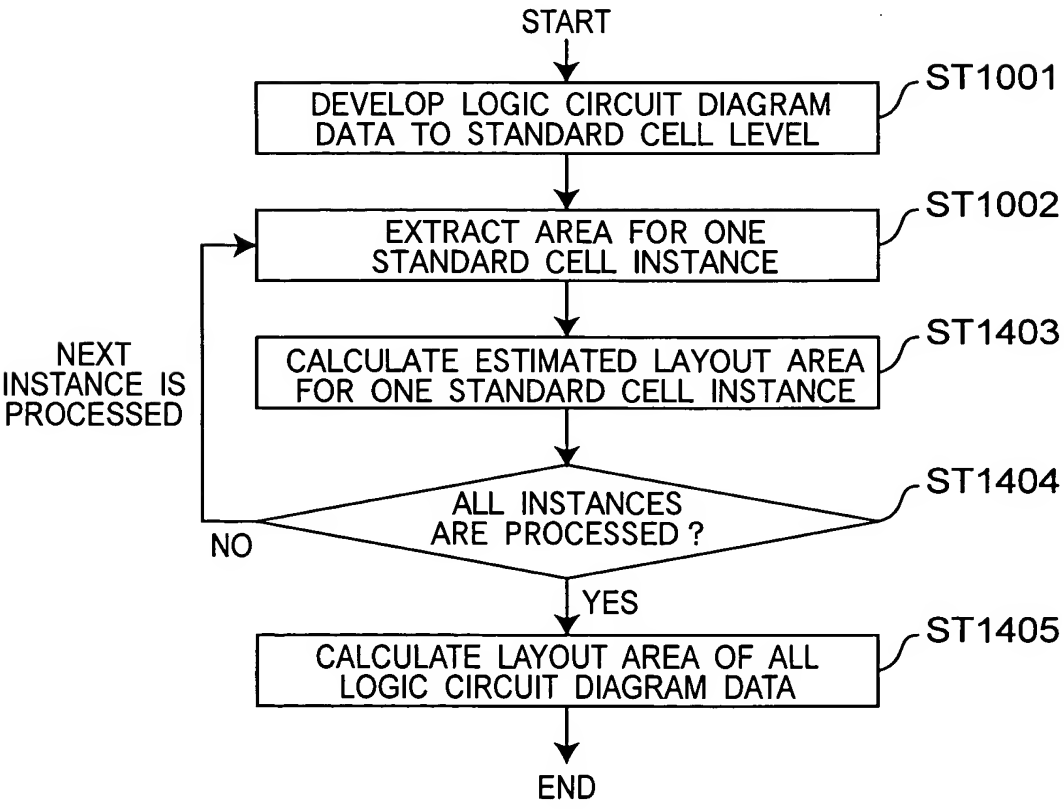


Fig.15

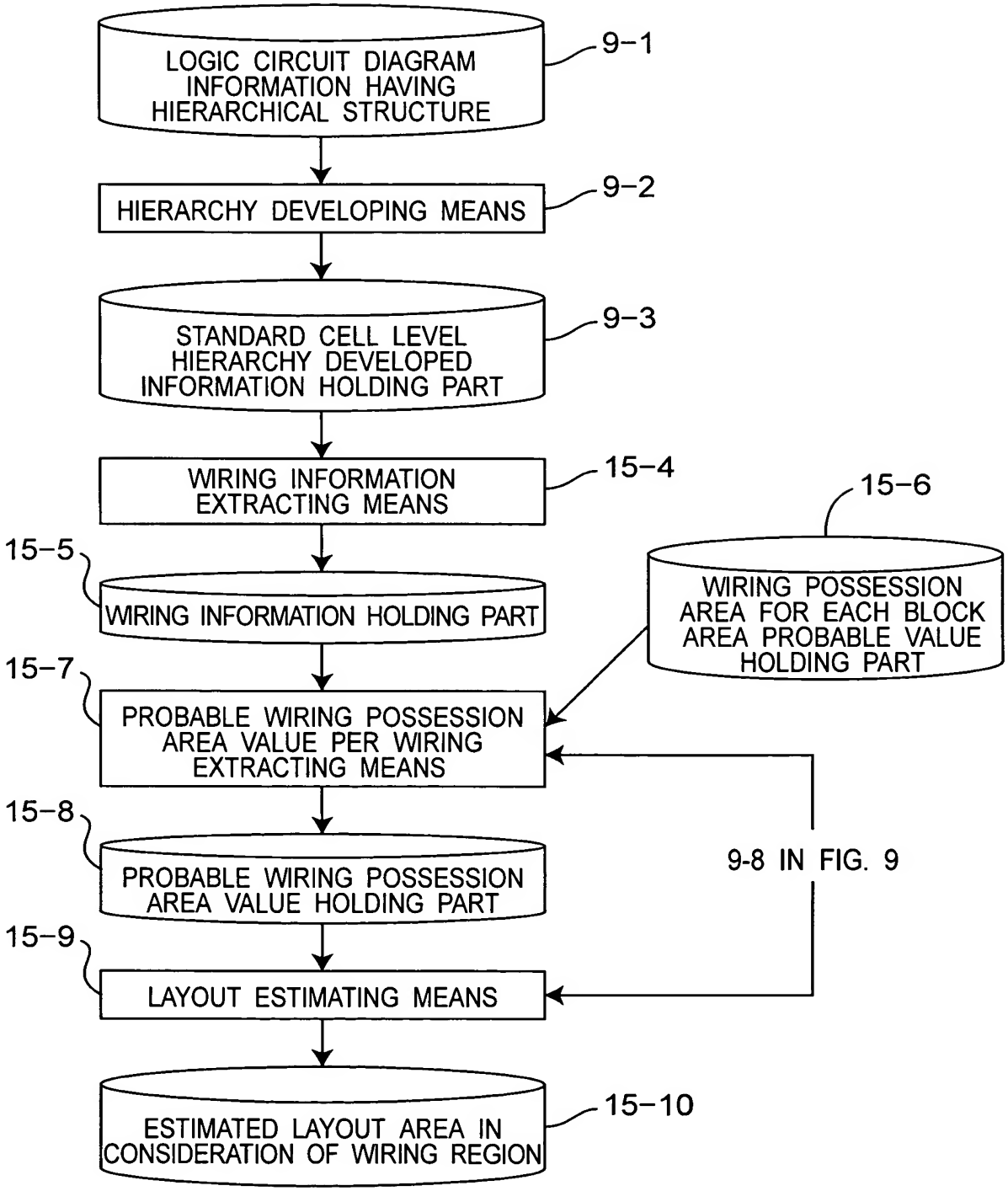

LOGIC CIRCUIT DIAGRAM INFORMATION HAVING HIERARCHICAL STRUCTURE
9-1
HIERARCHY DEVELOPING MEANS
9-2
STANDARD CELL LEVEL HIERARCHY DEVELOPED INFORMATION HOLDING PART
9-3
WIRING INFORMATION EXTRACTING MEANS
15-4
15-5
WIRING INFORMATION HOLDING PART
15-6
WIRING POSSESSION AREA FOR EACH BLOCK AREA PROBABLE VALUE HOLDING PART
15-7
PROBABLE WIRING POSSESSION AREA VALUE PER WIRING EXTRACTING MEANS
15-8
PROBABLE WIRING POSSESSION AREA VALUE HOLDING PART
9-8 IN FIG. 9
15-9
LAYOUT ESTIMATING MEANS
ESTIMATED LAYOUT AREA IN CONSIDERATION OF WIRING REGION
15-10

Fig.16

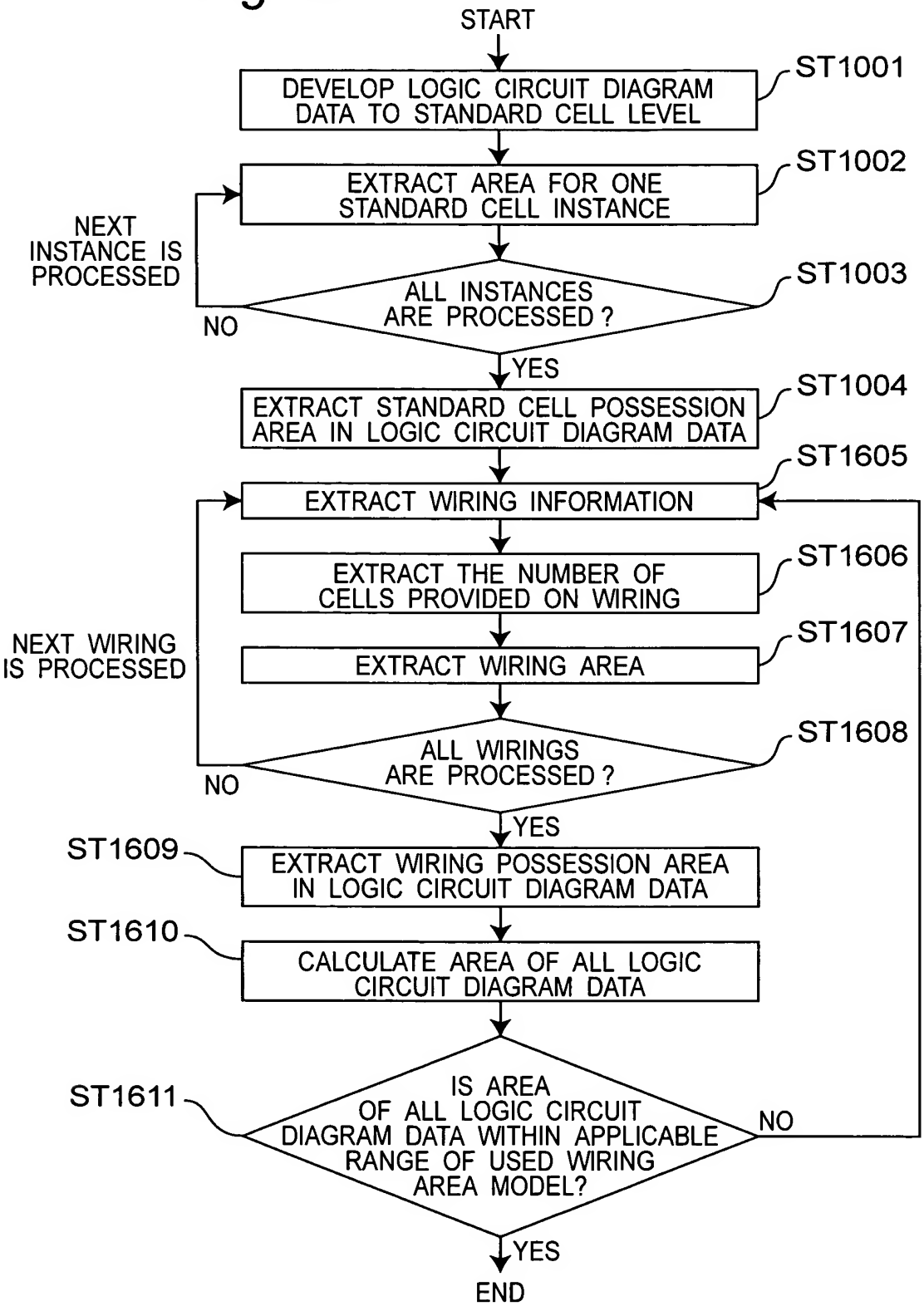

START
DEVELOP LOGIC CIRCUIT DIAGRAM DATA TO STANDARD CELL LEVEL
ST1001
EXTRACT AREA FOR ONE STANDARD CELL INSTANCE
ST1002
NEXT INSTANCE IS PROCESSED
ALL INSTANCES ARE PROCESSED ?
ST1003
NO
YES
EXTRACT STANDARD CELL POSSESSION AREA IN LOGIC CIRCUIT DIAGRAM DATA
ST1004
ST1605
EXTRACT WIRING INFORMATION
EXTRACT THE NUMBER OF CELLS PROVIDED ON WIRING
ST1606
NEXT WIRING IS PROCESSED
EXTRACT WIRING AREA
ST1607
ALL WIRINGS ARE PROCESSED ?
ST1608
NO
YES
ST1609
EXTRACT WIRING POSSESSION AREA IN LOGIC CIRCUIT DIAGRAM DATA
ST1610
CALCULATE AREA OF ALL LOGIC CIRCUIT DIAGRAM DATA
ST1611
IS AREA OF ALL LOGIC CIRCUIT DIAGRAM DATA WITHIN APPLICABLE RANGE OF USED WIRING AREA MODEL?
NO
YES
END

Fig.17

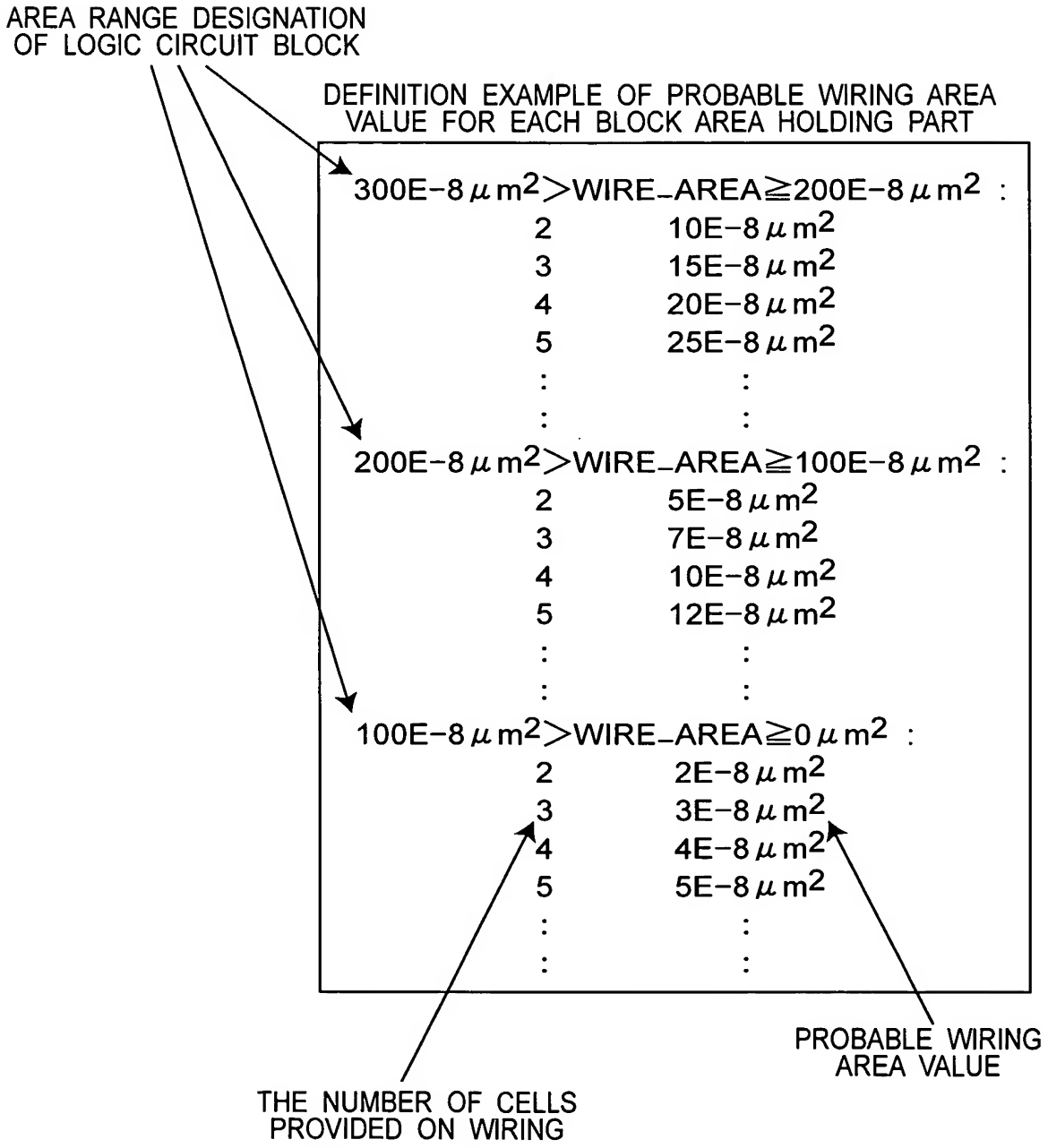

AREA RANGE DESIGNATION OF LOGIC CIRCUIT BLOCK
DEFINITION EXAMPLE OF PROBABLE WIRING AREA VALUE FOR EACH BLOCK AREA HOLDING PART
300E−8μm2>WIRE_AREA≧200E−8μm2 :
2 10E−8μm2
3 15E−8μm2
4 20E−8μm2
5 25E−8μm2
200E−8μm2>WIRE_AREA≧100E−8μm2 :
2 5E−8μm2
3 7E−8μm2
4 10E−8μm2
5 12E−8μm2
100E−8μm2>WIRE_AREA≧0μm2 :
2 2E−8μm2
3 3E−8μm2
4 4E−8μm2
5 5E−8μm2
PROBABLE WIRING AREA VALUE
THE NUMBER OF CELLS PROVIDED ON WIRING

Fig.18

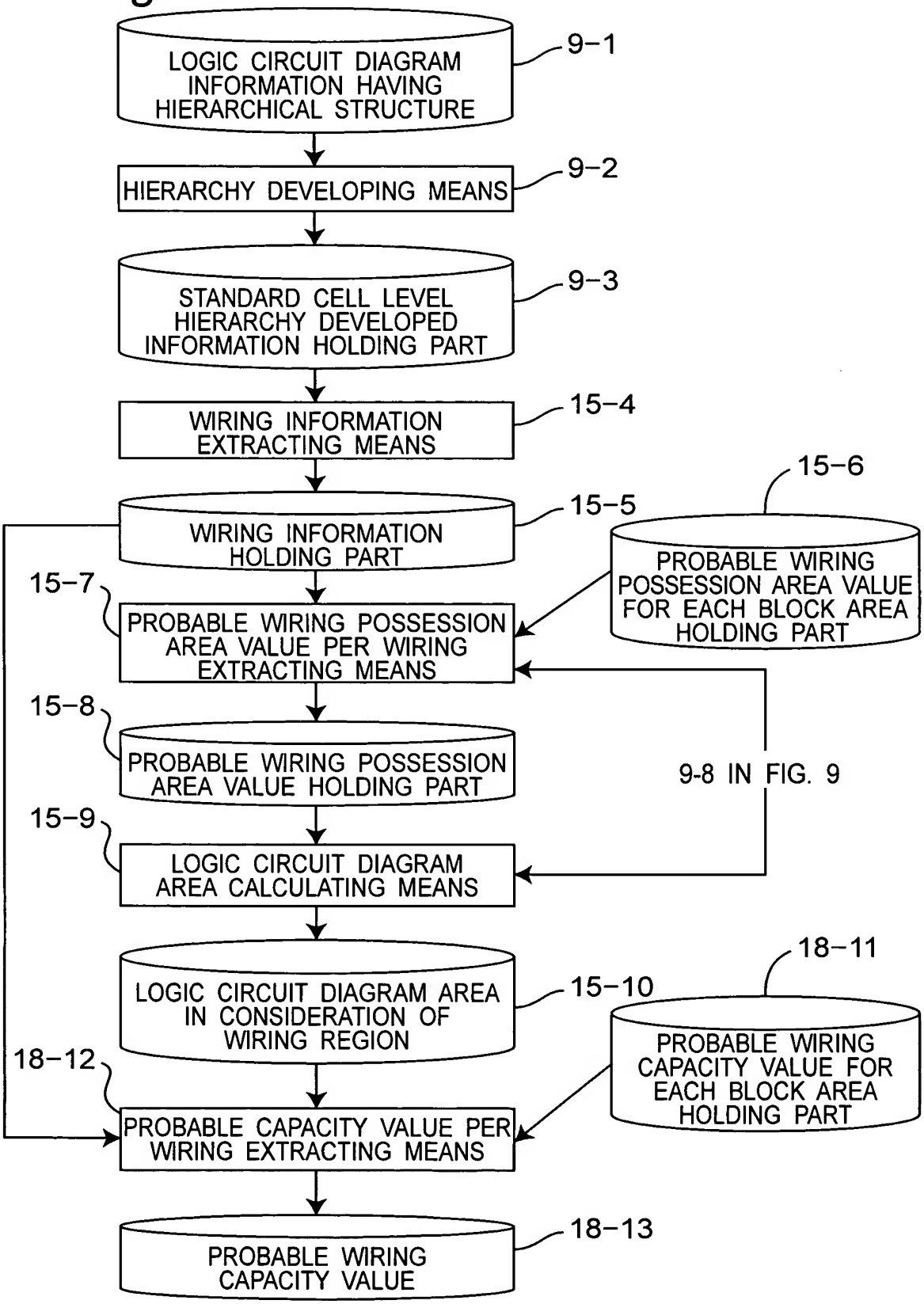

LOGIC CIRCUIT DIAGRAM INFORMATION HAVING HIERARCHICAL STRUCTURE
9-1
HIERARCHY DEVELOPING MEANS
9-2
STANDARD CELL LEVEL HIERARCHY DEVELOPED INFORMATION HOLDING PART
9-3
WIRING INFORMATION EXTRACTING MEANS
15-4
WIRING INFORMATION HOLDING PART
15-5
15-6
PROBABLE WIRING POSSESSION AREA VALUE FOR EACH BLOCK AREA HOLDING PART
15-7
PROBABLE WIRING POSSESSION AREA VALUE PER WIRING EXTRACTING MEANS
15-8
PROBABLE WIRING POSSESSION AREA VALUE HOLDING PART
9-8 IN FIG. 9
15-9
LOGIC CIRCUIT DIAGRAM AREA CALCULATING MEANS
LOGIC CIRCUIT DIAGRAM AREA IN CONSIDERATION OF WIRING REGION
15-10
18-11
PROBABLE WIRING CAPACITY VALUE FOR EACH BLOCK AREA HOLDING PART
18-12
PROBABLE CAPACITY VALUE PER WIRING EXTRACTING MEANS
PROBABLE WIRING CAPACITY VALUE
18-13

Fig.19

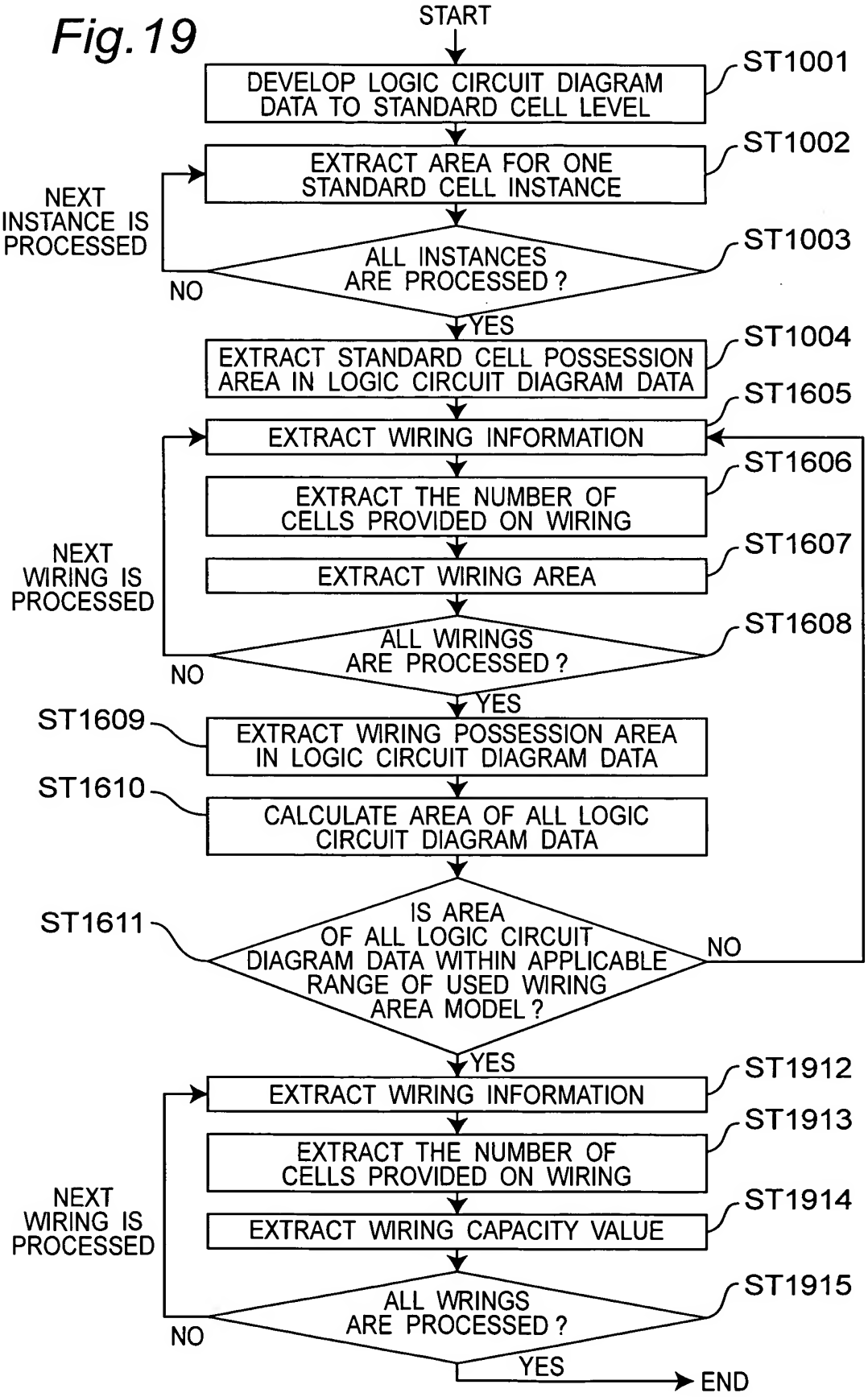

START
DEVELOP LOGIC CIRCUIT DIAGRAM DATA TO STANDARD CELL LEVEL
ST1001
EXTRACT AREA FOR ONE STANDARD CELL INSTANCE
ST1002
NEXT INSTANCE IS PROCESSED
ALL INSTANCES ARE PROCESSED ?
ST1003
NO
YES
EXTRACT STANDARD CELL POSSESSION AREA IN LOGIC CIRCUIT DIAGRAM DATA
ST1004
ST1605
EXTRACT WIRING INFORMATION
ST1606
EXTRACT THE NUMBER OF CELLS PROVIDED ON WIRING
ST1607
NEXT WIRING IS PROCESSED
EXTRACT WIRING AREA
ALL WIRINGS ARE PROCESSED ?
ST1608
NO
YES
ST1609
EXTRACT WIRING POSSESSION AREA IN LOGIC CIRCUIT DIAGRAM DATA
ST1610
CALCULATE AREA OF ALL LOGIC CIRCUIT DIAGRAM DATA
ST1611
IS AREA OF ALL LOGIC CIRCUIT DIAGRAM DATA WITHIN APPLICABLE RANGE OF USED WIRING AREA MODEL ?
NO
YES
ST1912
EXTRACT WIRING INFORMATION
ST1913
EXTRACT THE NUMBER OF CELLS PROVIDED ON WIRING
ST1914
NEXT WIRING IS PROCESSED
EXTRACT WIRING CAPACITY VALUE
ALL WRINGS ARE PROCESSED ?
ST1915
NO
YES
END

Fig.20

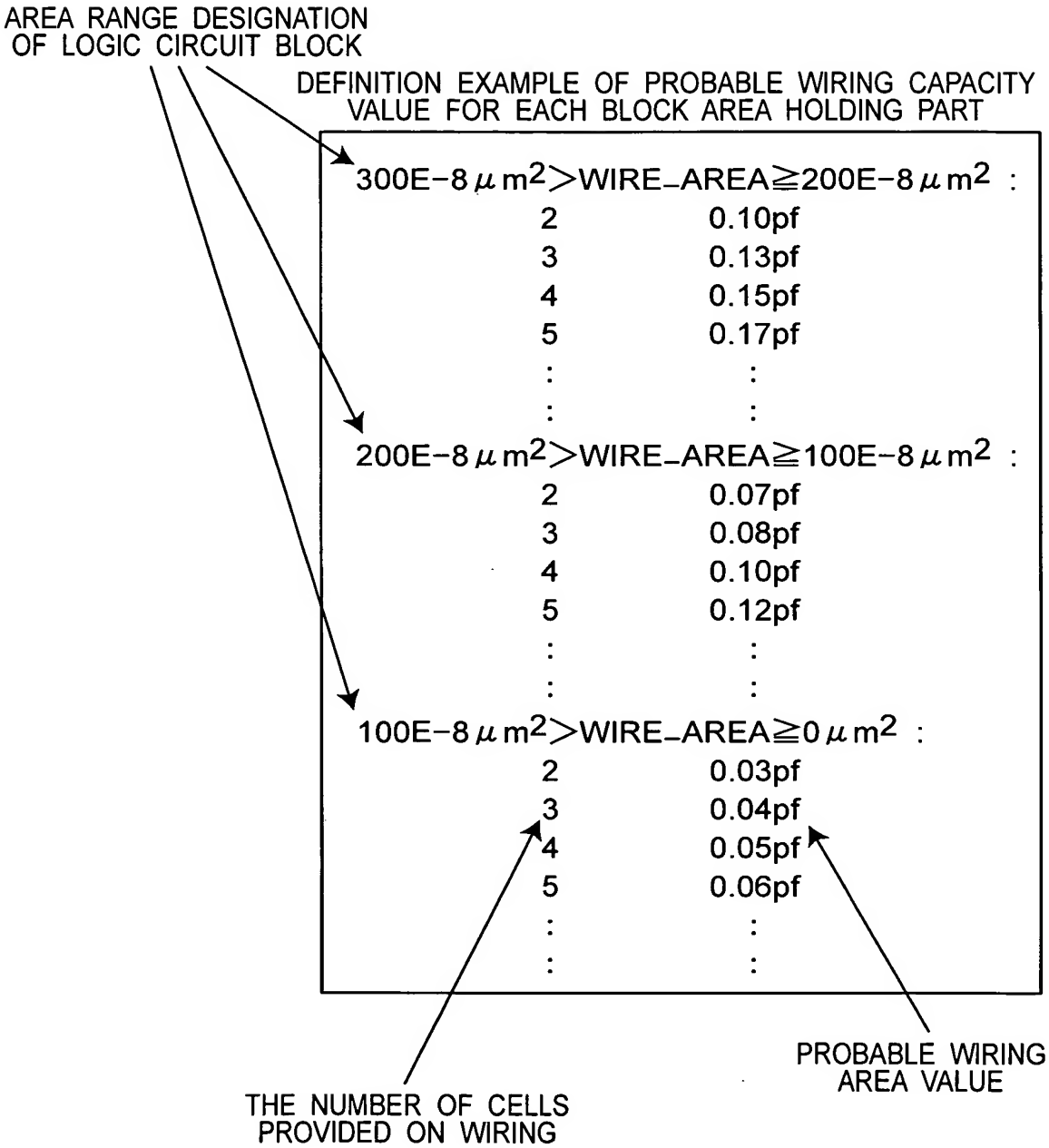

AREA RANGE DESIGNATION OF LOGIC CIRCUIT BLOCK
DEFINITION EXAMPLE OF PROBABLE WIRING CAPACITY VALUE FOR EACH BLOCK AREA HOLDING PART
300E−8 μm2>WIRE_AREA≧200E−8 μm2 :
2 0.10pf
3 0.13pf
4 0.15pf
5 0.17pf
200E−8 μm2>WIRE_AREA≧100E−8 μm2 :
2 0.07pf
3 0.08pf
4 0.10pf
5 0.12pf
100E−8 μm2>WIRE_AREA≧0 μm2 :
2 0.03pf
3 0.04pf
4 0.05pf
5 0.06pf
THE NUMBER OF CELLS PROVIDED ON WIRING
PROBABLE WIRING AREA VALUE

Fig.21

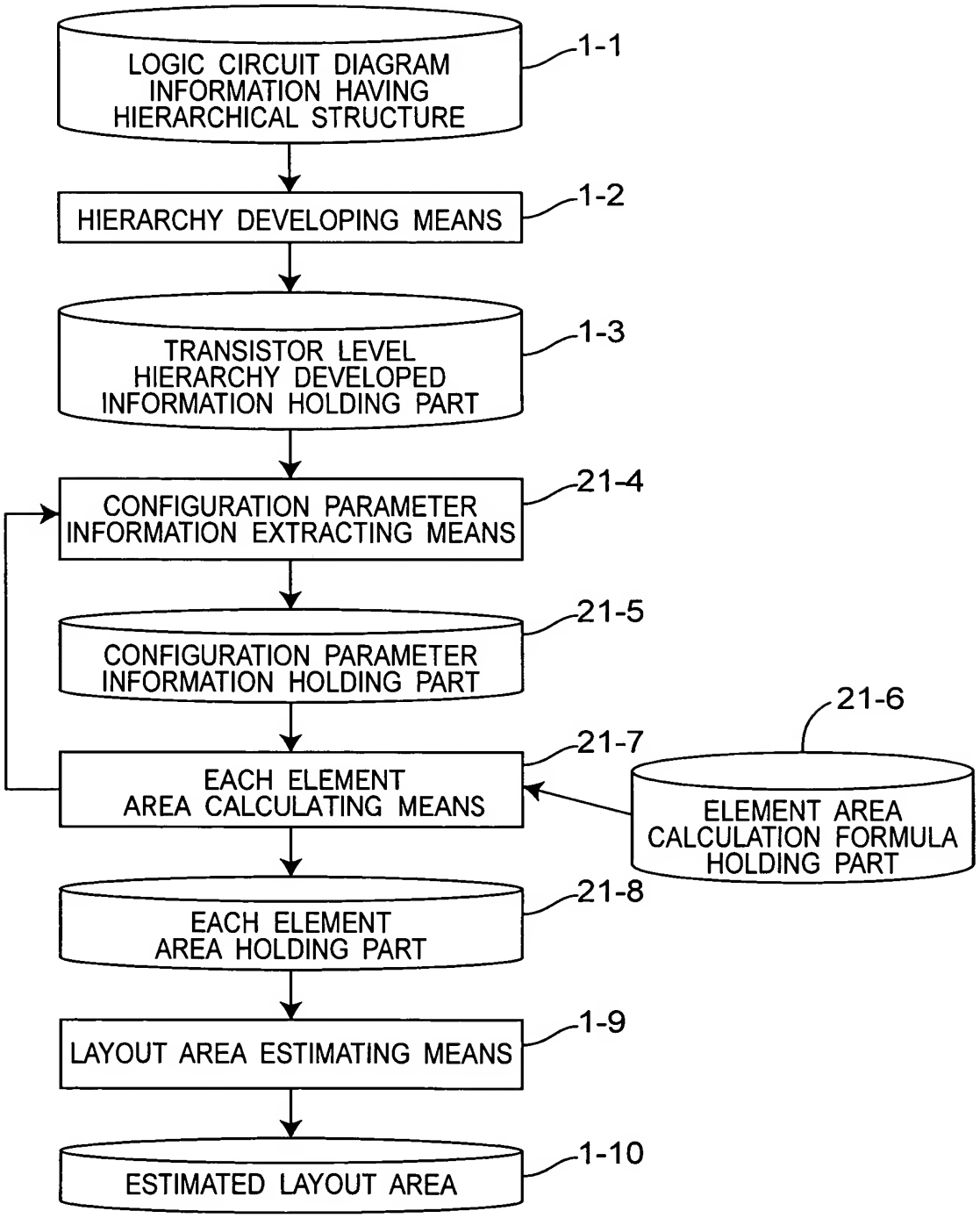

LOGIC CIRCUIT DIAGRAM INFORMATION HAVING HIERARCHICAL STRUCTURE
1-1
HIERARCHY DEVELOPING MEANS
1-2
TRANSISTOR LEVEL HIERARCHY DEVELOPED INFORMATION HOLDING PART
1-3
CONFIGURATION PARAMETER INFORMATION EXTRACTING MEANS
21-4
CONFIGURATION PARAMETER INFORMATION HOLDING PART
21-5
21-6
EACH ELEMENT AREA CALCULATING MEANS
21-7
ELEMENT AREA CALCULATION FORMULA HOLDING PART
EACH ELEMENT AREA HOLDING PART
21-8
LAYOUT AREA ESTIMATING MEANS
1-9
ESTIMATED LAYOUT AREA
1-10

Fig.22

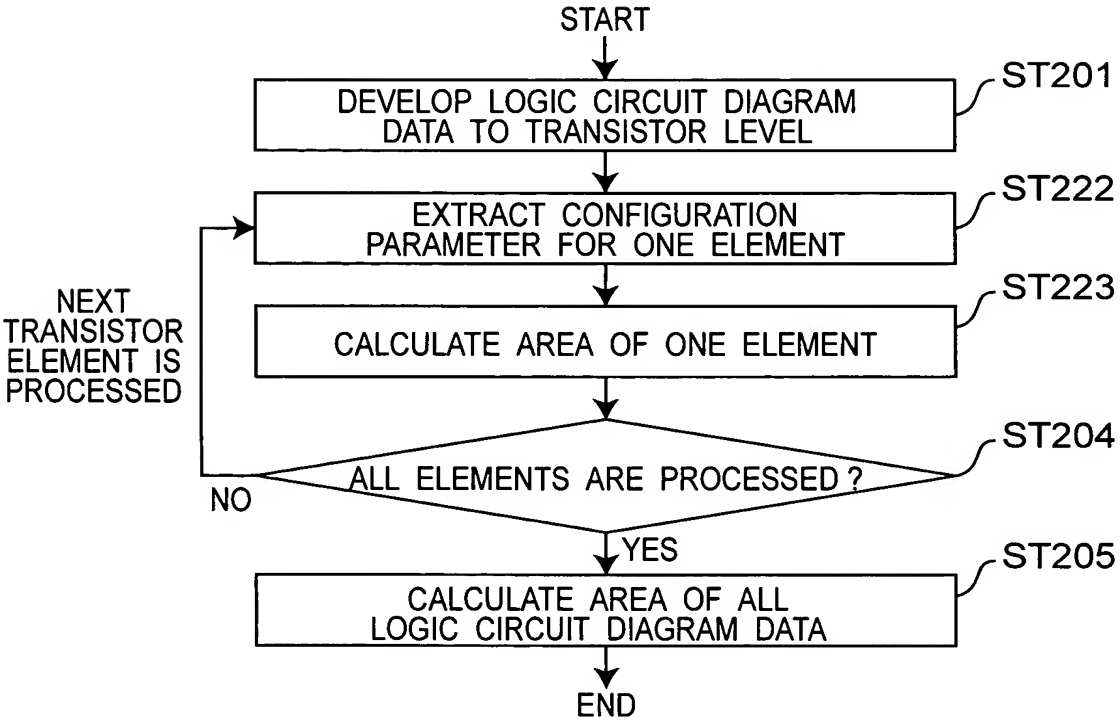
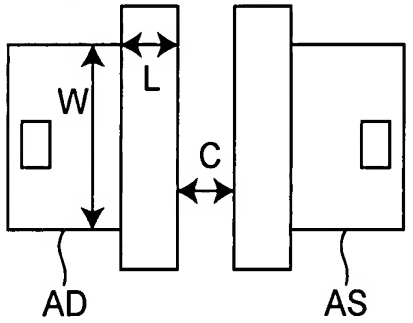

START
DEVELOP LOGIC CIRCUIT DIAGRAM DATA TO TRANSISTOR LEVEL
ST201
EXTRACT CONFIGURATION PARAMETER FOR ONE ELEMENT
ST222
CALCULATE AREA OF ONE ELEMENT
ST223
NEXT TRANSISTOR ELEMENT IS PROCESSED
ALL ELEMENTS ARE PROCESSED ?
ST204
NO
YES
CALCULATE AREA OF ALL LOGIC CIRCUIT DIAGRAM DATA
ST205
END

Fig.23

CONFIGURATION PARAMETER OF TRANSISTOR



L : GATE LENGTH
W : GATE WIDTH
AD : DRAIN REGION AREA
AS : SOURCE REGION AREA
D : DISTANCE BETWEEN GATES
M : THE NUMBER OF GATES

PARAMETER OF RESISTANCE : RESISTANCE VALUE
PARAMETER OF CAPACITY : CAPACITY VALUE

Fig.24

TRANSISTOR AREA CALCULATION FORMULA HOLDING PART

ONE TRANSISTOR AREA = $L \times W \times M + AD + AS + D \times W$

AREA OF ONE RESISTANCE = [RESISTANCE VALUE] / [RESISTANCE VALUE PER UNIT LENGTH] x [WIRING WIDTH]

AREA OF ONE CAPACITY = [CAPACITY VALUE] / [CAPACITY VALUE PER UNIT LENGTH] x [WIRING WIDTH]

Fig.25

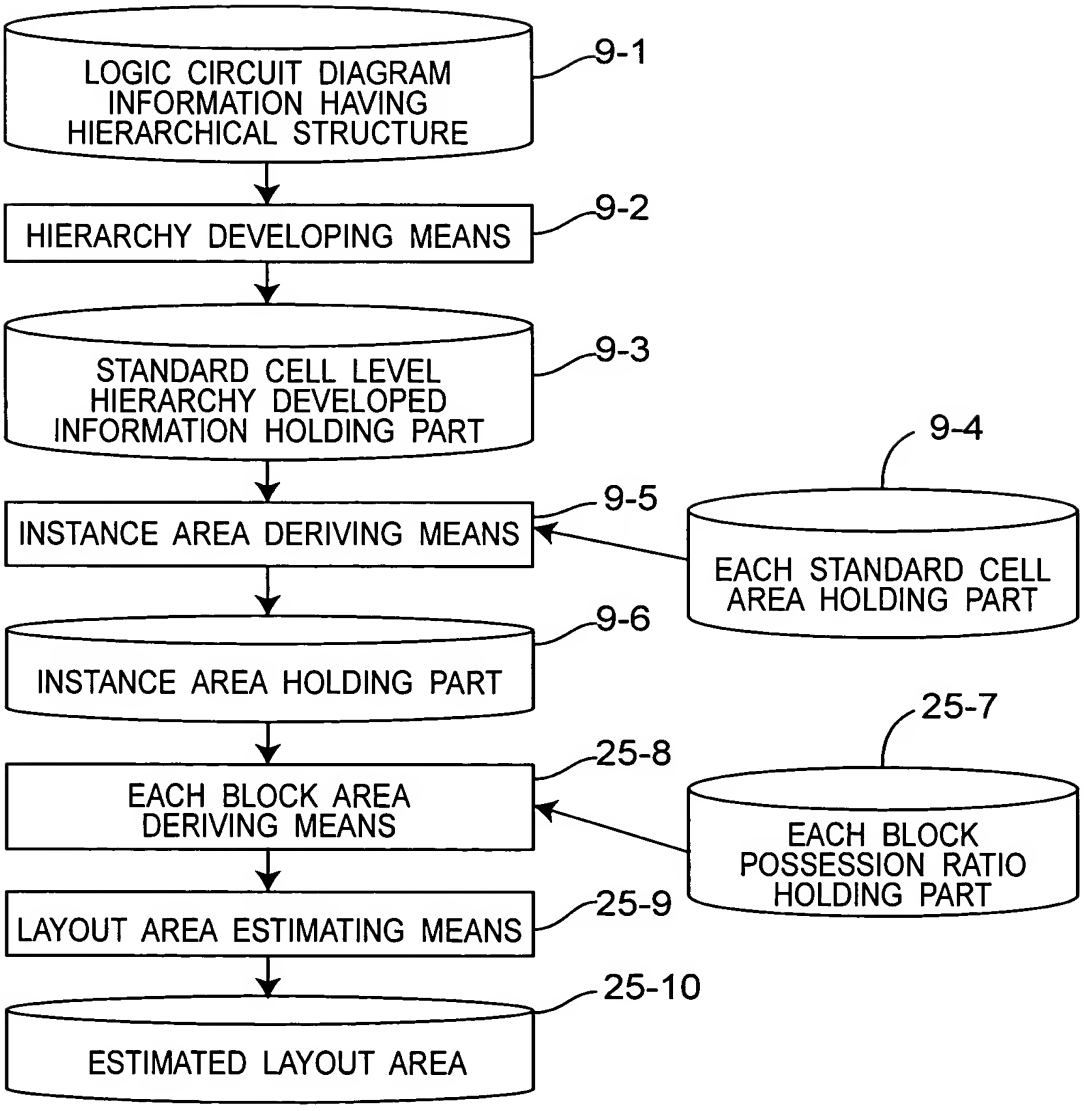
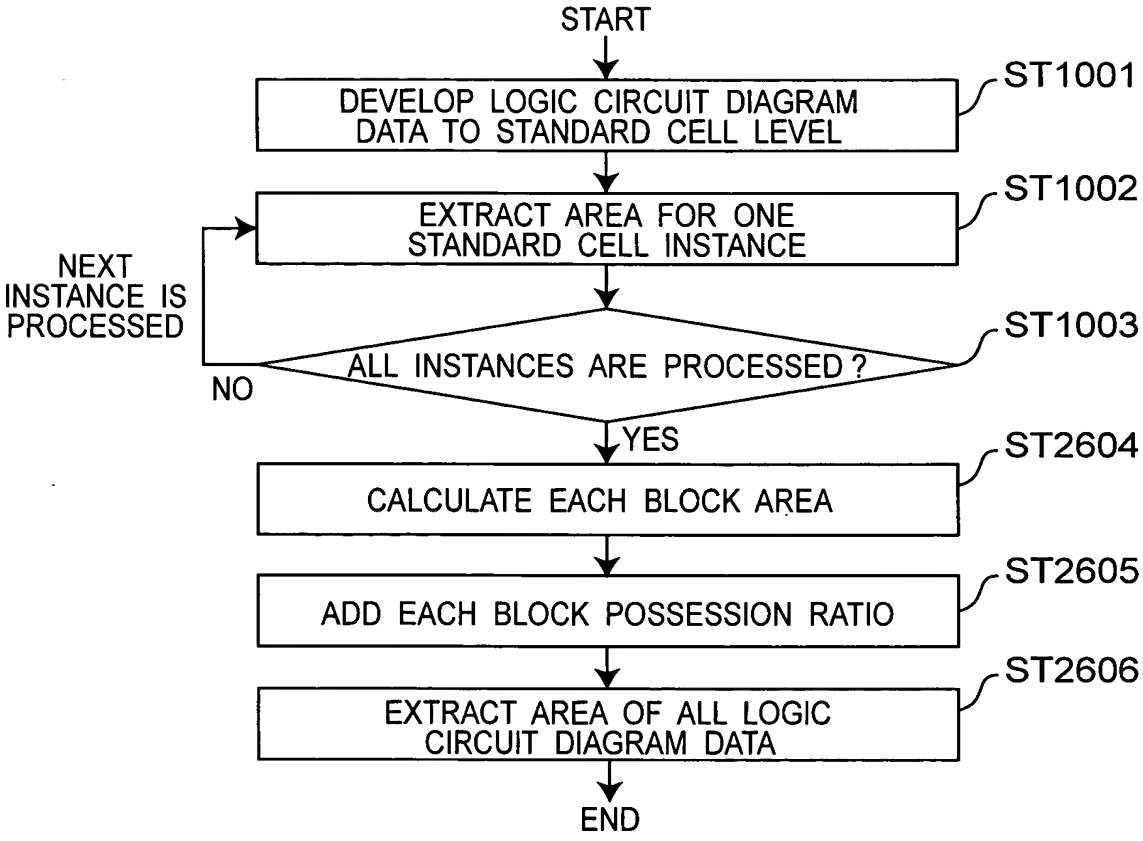

LOGIC CIRCUIT DIAGRAM INFORMATION HAVING HIERARCHICAL STRUCTURE
9-1
HIERARCHY DEVELOPING MEANS
9-2
STANDARD CELL LEVEL HIERARCHY DEVELOPED INFORMATION HOLDING PART
9-3
9-4
INSTANCE AREA DERIVING MEANS
9-5
EACH STANDARD CELL AREA HOLDING PART
INSTANCE AREA HOLDING PART
9-6
25-7
EACH BLOCK AREA DERIVING MEANS
25-8
EACH BLOCK POSSESSION RATIO HOLDING PART
LAYOUT AREA ESTIMATING MEANS
25-9
ESTIMATED LAYOUT AREA
25-10

Fig.26


START
DEVELOP LOGIC CIRCUIT DIAGRAM DATA TO STANDARD CELL LEVEL
ST1001
EXTRACT AREA FOR ONE STANDARD CELL INSTANCE
ST1002
NEXT INSTANCE IS PROCESSED
ALL INSTANCES ARE PROCESSED ?
ST1003
NO
YES
CALCULATE EACH BLOCK AREA
ST2604
ADD EACH BLOCK POSSESSION RATIO
ST2605
EXTRACT AREA OF ALL LOGIC CIRCUIT DIAGRAM DATA
ST2606
END